1. DESCRIPTION

The IL1520B family of dot matrix LCD (Liquid Crystal Display) drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM. The IL1520B family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems. The IL1520B which is able to drive two lines of twelve characters each.

2. FEATURES

- CMOS LSI chips
- Connection with CPU
- Can be directly coupled with 80-port or 68-port system
- Available in chip form or in 100-pin plastic QFP
- Pin-to-Pin Replacement for SED1520 Series
- Many command set
- Total 80 (segment+common) drive sets
- Low power consumption - 30μW maximum at 2kHz external clock
- Power supply V_{DD} - V_{SS} : 2.4 to -7.0V
  V_{DD} - V_5 : 3.5 to -13.0V

3. ABSOLUTE MAXIMUM RATINGS

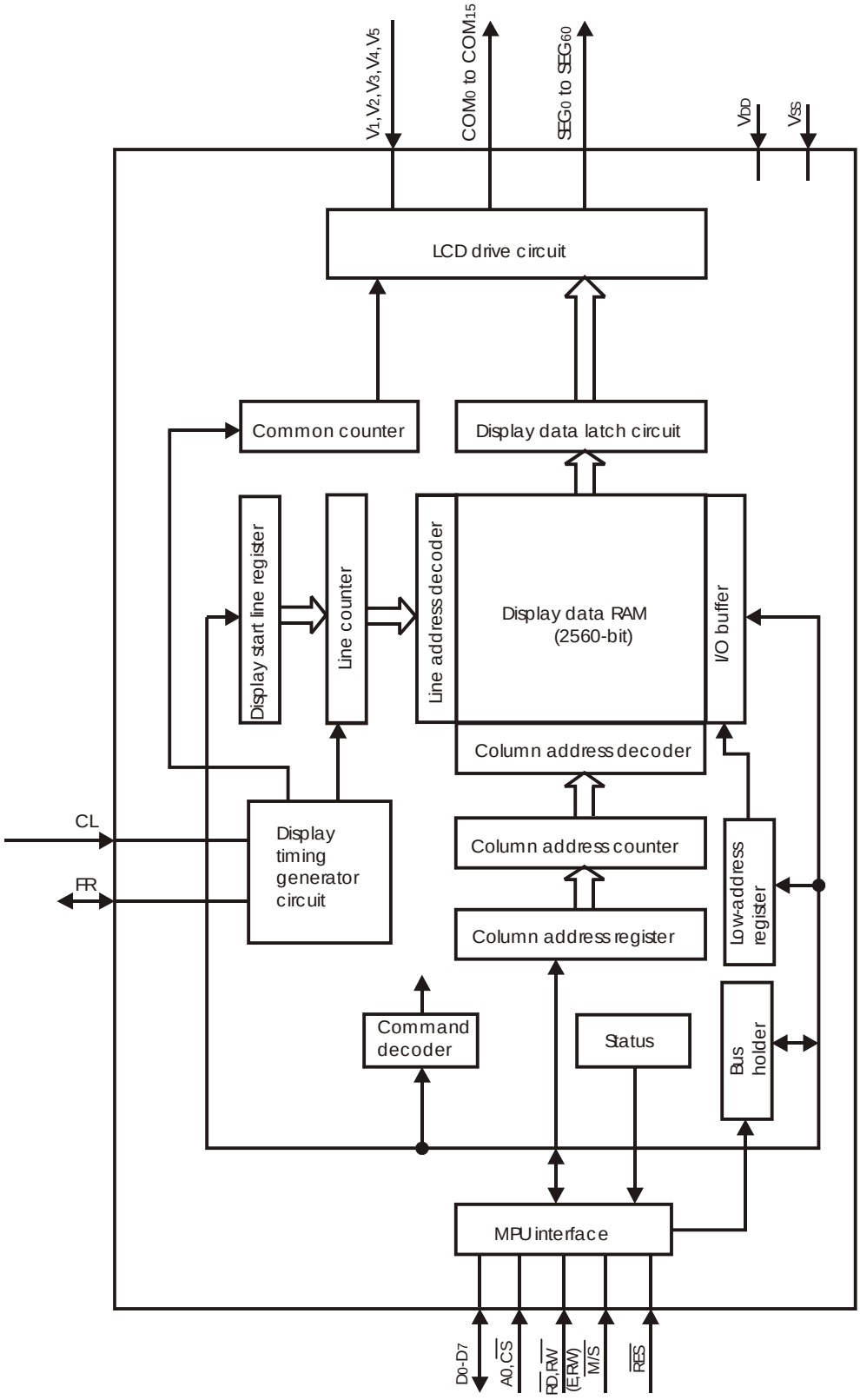
Characteristic	Symbol	Value	Unit
Supply Voltage (1)	V_{SS}	- 8.0 ~ 0.3	V
Supply Voltage (2)	V_5	- 16.5 ~ 0.3	V
Supply Voltage (3)	V_1, V_2, V_3, V_4	V_5 ~ 0.3	V
Input Voltage	V_I	V_{SS} - 0.3 ~ 0.3	V
Output Voltage	V_O	V_{SS} - 0.3 ~ 0.3	V
Power Dissipation	P_D	250	mW
Operating Temperature	T_a	- 20 ~ + 75	°C
Storage Temperature	T_{stg}	- 55 ~ + 125	°C
Soldering temperature time (10 sec max)	T_{sol}	260	°C

Notes:
1. All voltages are specified relative to V_{DD} = 0V.
2. The following relation must be always hold $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operating under these conditions is not implied.

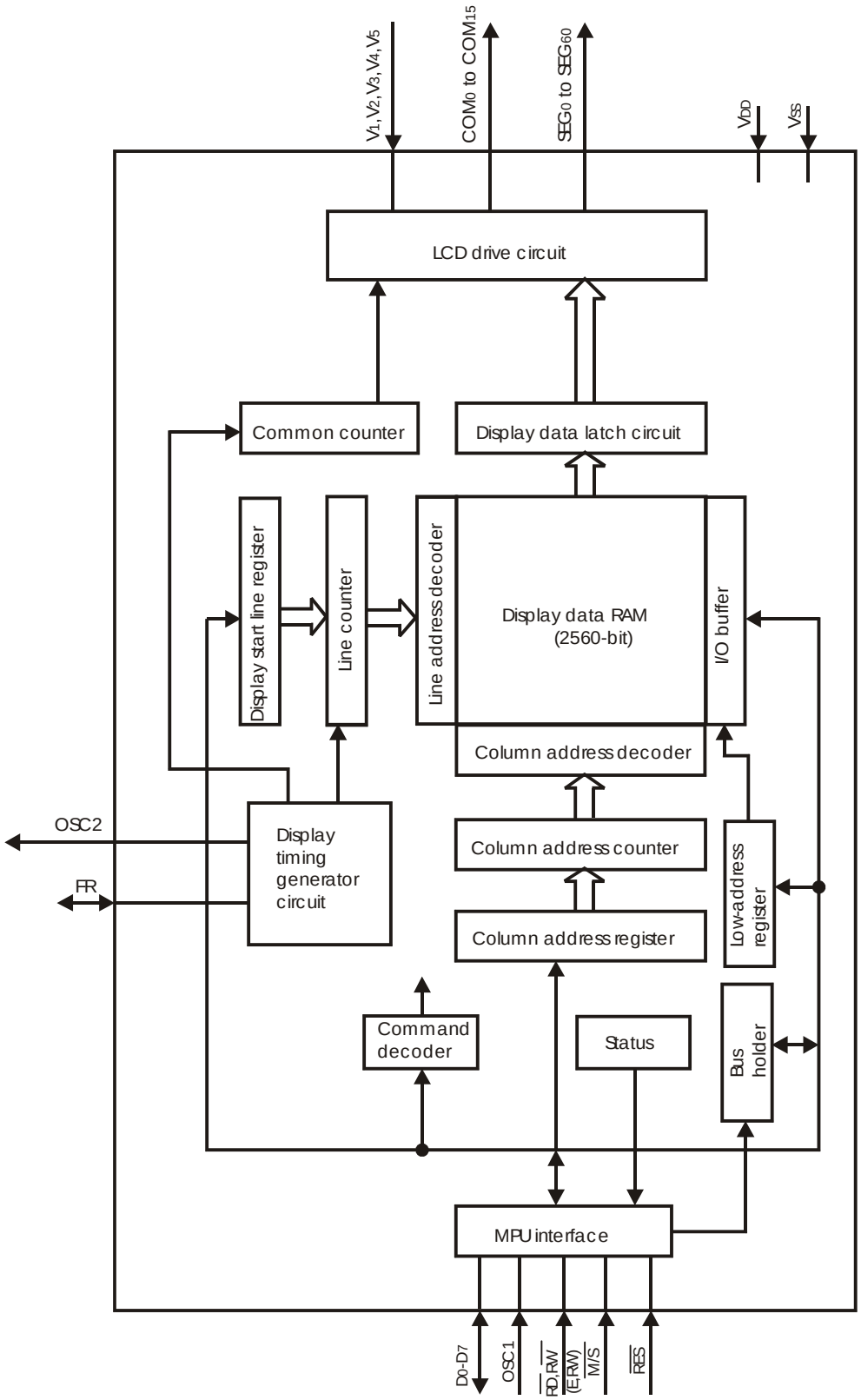
4. LINE-UP

Product Name	Clock Frequency		Applicable Driver	Number of SEGMENT Drivers	Number of COMMON Drivers	Duty
	On-chip	External				
IL1520B $_{OA}$	18kHz	18kHz	IL1520B $_{OA}$, IW1521$_{OA}$	61	16	1/16, 1/32
IL1520B $_{AA}$	-	2kHz	IL1520B $_{AA}$, IW1521$_{AA}$	61	16	1/16, 1/32

5. BLOCK DIAGRAM IL1520B AA



6. BLOCK DIAGRAM IL1520B OA



7. ELECTRICAL CHARACTERISTICS (Ta = -20 to 75°C, V_{DD} = 0V, V_{SS} = -5.0V unless otherwise specified)

Characteristic		Symbol	Test Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating Voltage(1) Note 1	Recommended	V_{SS}		V_{SS}	-5.5	-5.0	-4.5	V
					-7.0		-2.4	
Operating Voltage(2)	Recommended	V_5		V_5	-13.0		-3.5	V
					-13.0			
	Permitted	V_1, V_2		V_1, V_2	0.6 x V_5		V_{DD}	
	Permitted	V_3, V_4		V_3, V_4	V_5		0.4xV_5	
HIGH Input Voltage		V_{IH}		A0,Di, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}+2.0		V_{DD}	V
				CL, FR, M/$\overline{S}$, $\overline{RES}$	0.2 x V_{SS}		V_{DD}	
LOW Input Voltage		V_{IL}		A0, Di, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}		V_{SS}+0.8	V
				CL, FR, M/$\overline{S}$, $\overline{RES}$	V_{SS}		0.8+V_{SS}	
HIGH Output Voltage		V_{OH}	I_{OH} = -3.0 mA	D0 ÷ D7	V_{SS}+2.4			V
			I_{OH} = -2.0 mA	FR	V_{SS}+2.4			
			I_{OH} = -120 µA	OSC2	0.2 x V_{SS}			
LOW Output Voltage		V_{OL}	I_{OL} = 3.0 mA	D0 ÷ D7			V_{SS}+0.4	V
			I_{OL} = 2.0 mA	FR			V_{SS}+0.4	
			I_{OL} = 120µA	OSC2			0.8xV_{SS}	
Input Leakage Current		I_{LI}		A0, E, R/W, $\overline{CS}$, $\overline{CL}$, M/$\overline{S}$, $\overline{RES}$	-1.0		1.0	µA
Output Leakage Current		I_{LO}	Outputs are high impedance	D0 ÷ D7, FR	-3.0		3.0	µA
LCD Driver ON Resistance Note 2		R_{ON}	V_5=-5.0V	SEG0 ~ SEG79 COM0 ~ COM15		5.0	7.5	kΩ
Supply Current, Static		I_{DDQ}	$\overline{CS}$ = CL = V_{DD}	V_{DD}		0.05	1.0	µA
Supply Current, Dynamic		I_{DD}	During display V_5=-5.0V, f_{CL}=2kHz Note 3	V_{DD}		2.0	5.0	µA
			During display V_5=-5.0V, R_f =1MΩ Note 4			9.5	15.0	
			During display V_5=-5.0V, f_{CL}=18kHz Note 5			5.0	10.0	
			During access f_{cyc}=200kHz			300	500	µA
Input Terminal Capacity		C_{IN}	f = 1 MHz	All inputs		5.0	8.0	pF
Oscillator Frequency		f_{OSC}	R_f =1MΩ±2%		15	18	21	kHz
Reset Time		t_R		RES	1.0		1000	µs

Notes:
1. Operating over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. For a voltage differential of 0.1V between input (V_1, …, V_4) and output (COM, SEC) pins. All voltages within specified operating voltage range.
3. IL1520B $_{AA}$ does not include transient currents due to stray and panel capacitances.
4. IL1520B $_{OA}$ only. Does not include transient currents due to stray and panel capacitances.

• Read/Write timing for the 80-port MPU

Characteristic	Symbol	Signal	Condition	Min	Typ	Max	Unit
Address hold time	t_{AH8}	A0, $\overline{CS}$	CL = 100pF	10			ns
Address setup time	t_{AW8}			20			ns
System cycle time	t_{CYC8}	$\overline{WR}$, $\overline{RD}$		1000			ns
Control pulse width	t_{CC8}			200			ns
Data setup time	t_{DS8}	D0 ÷ D7		80			ns
Data hold time	t_{DH8}			10			ns
V_{DD} access time	t_{ACC8}					90	ns
Output Disable time	t_{OH8}			10		60	ns
Low-level pulsewidth	t_{WLCL}	CL		35			µs
High-level pulsewidth	t_{WHCL}			35			µs
Rise time	t_r				30	150	ns
Fall time	t_f				30	150	ns
FR delay time Note 1	t_{FDR}	FR (Input)		-2.0	0.2	2.0	µs
FR delay time Note 2	t_{FDR}	FR (Input)			0.2	2.0	µs

• Read/Write timing for the 68-port MPU

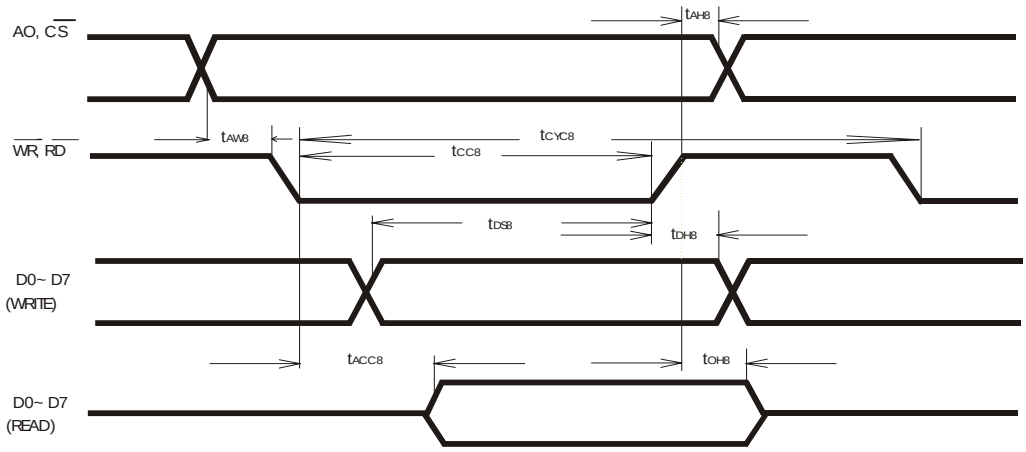
Characteristic		Symbol	Signal	Condition	Min	Typ	Max	Unit
System cycle time		t_{CYC6}	A0	CL = 100pF	1000			ns
Address setup time		t_{AW6}	R/W		20			ns
Address hold time		t_{AH6}			10			ns
Data setup time		t_{DS6}	D0 ÷ D7		80			ns
Data hold time		t_{DH6}			10			ns
Output disable time		t_{OH6}			10		60	ns
Access time		t_{ACC6}					90	ns
Enable pulse width	READ	t_{EW}	E		100			ns
	WRITE				80			ns
Low-level pulsewidth		t_{WLCL}	CL		35			µs
High-level pulsewidth		t_{WHCL}			35			µs
Rise time		t_r				30	150	ns
Fall time		t_f				30	150	ns
FR delay time Note 1		t_{FDR}	FR (Input)		-2.0	0.2	2.0	µs
FR delay time Note 2		t_{FDR}	FR (Input)			0.2	2.0	µs

* The rating when V_{SS} = -3.0V are approximately 100% higher that when V_{SS} = -5.0V

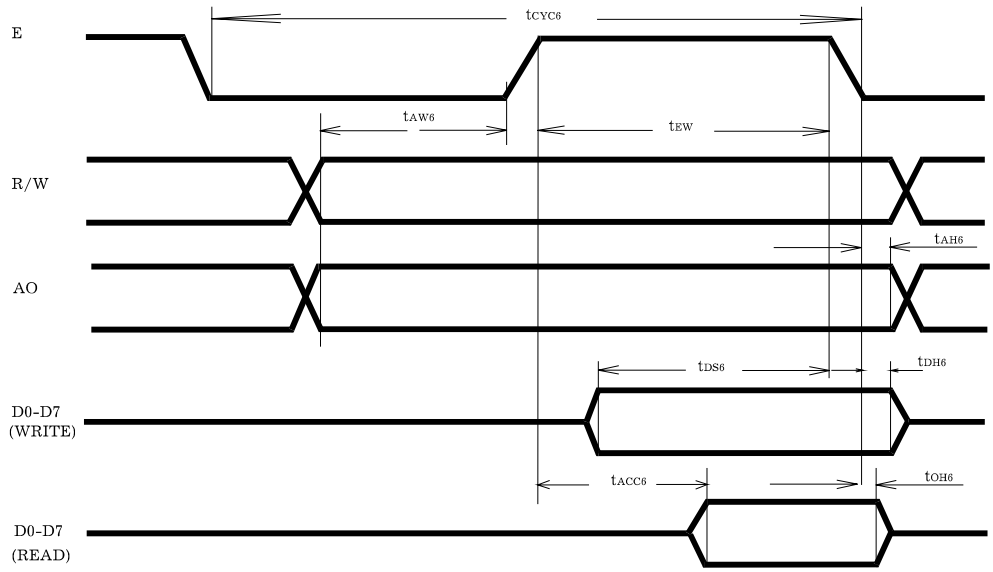
Notes: 1. The listed input t_{FDR} applies to IL1520B in slave mode.
2. The listed input t_{FDR} applies to IL1520B in master mode.

• **Timing Chart**

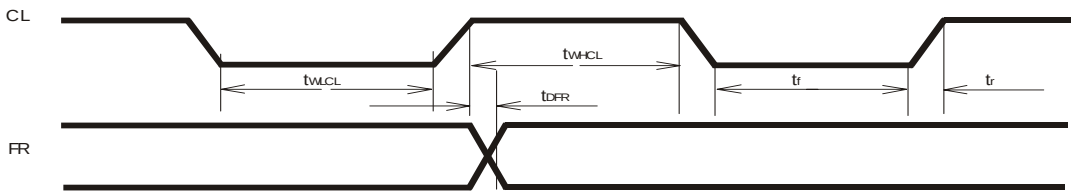
• **Read/Write timing for the 80-port MPU**



• **Read/Write timing for the 68-port MPU**



• **Read/Write timing for the 80-port/68-port display**



TERMINAL DESCRIPTION

Terminal Name	Function
D0 ÷ D7	Data I/O
A0	Select display data or functions. HIGH: Display data LOW : Instructions
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU HIGH: 68-port MPU interface LOW : 80-port MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only.
OSC1	Chip Select input LOW : Active level sensing
E ($\overline{RD}$)	Read/Write Enable signal when a 68-port MPU is connected. (Active LOW Read Enable signal when an 80-port MPU is connected)
R/W ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW : Write Select (Active LOW Write Enable input when an 80-port MPU is connected Rising edge sensing)
$\overline{CL}$	Input. Effective for an external clock operation model only.
OSC2	External clock input (only effective with external clock types)
FR	LCD Frame (AC- conversion) signal input/output
SEGn	Segment output for driving the LCD
COMn	Common output for driving the LCD
M/S	Master/Slave Select signal
V_{DD}	5V power supply
V_{SS}	0V power supply (GND level)
V_1, V_2, V_3, V_4, V_5	Power supplies for driving the LCD. $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

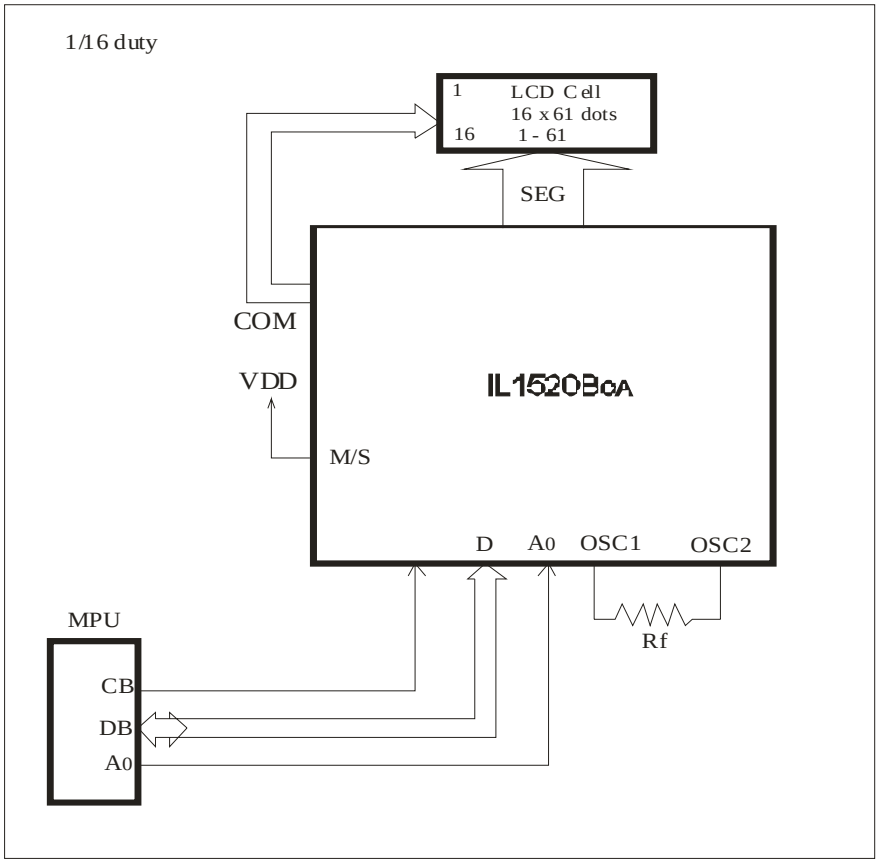
DISPLAY COMMANDS (Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU)

	Command	RD	WR	A0	D7	D6	D5	D4	D3	D2	D1 D0	Function	
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1 0/1	Switches the entire display ON or OFF regardless of the Display RAM's data or the internal status. *Note	
2	Display START Line	1	0	0	1	1	0	Display START address (0 ÷ 31)				Determines the line of RAM data to be displayed at the display's top line (COM0)	
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page	Sets the page of the Display RAM in the page address register	
4	Column (Segment) Address Set	1	0	0	0	Column address (0 ÷ 79)						Sets the column address of the Display RAM in the column address register	
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0 0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal	
6	Write Display Data	1	0	1	Write Data							Writes the data on the data bus to RAM	These commands access a previously specified address
7	Read Display Data	0	1	1	Read Data							Reads data from the Display RAM onto the data bus	of the Display RAM, after which the column address is incremented one
8	ADC Select	1	0	0	1	0	1	0	0	0	0 0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse)	
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0 0/1	Selects normal display operation or static all-fit drive display operation 1: Static drive (Power Save) 0: Normal display	
10	Duty Select	1	0	0	1	0	1	0	1	0	0 0/1	Selects the duty factor for driving LCD cells 1: 1/32 duty 0: 1/16 duty	
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0 0	Increments the column address counter by one only when display data is written but not when it is read	
12	End	1	0	0	1	1	1	0	1	1	1 0	Cancels the Ready Modify Write mode	
13	Reset	1	0	0	1	1	1	0	0	0	1 0	Resets the Display START line to the 1-st line in the register. Resets the column address counter and page address register to 0.	

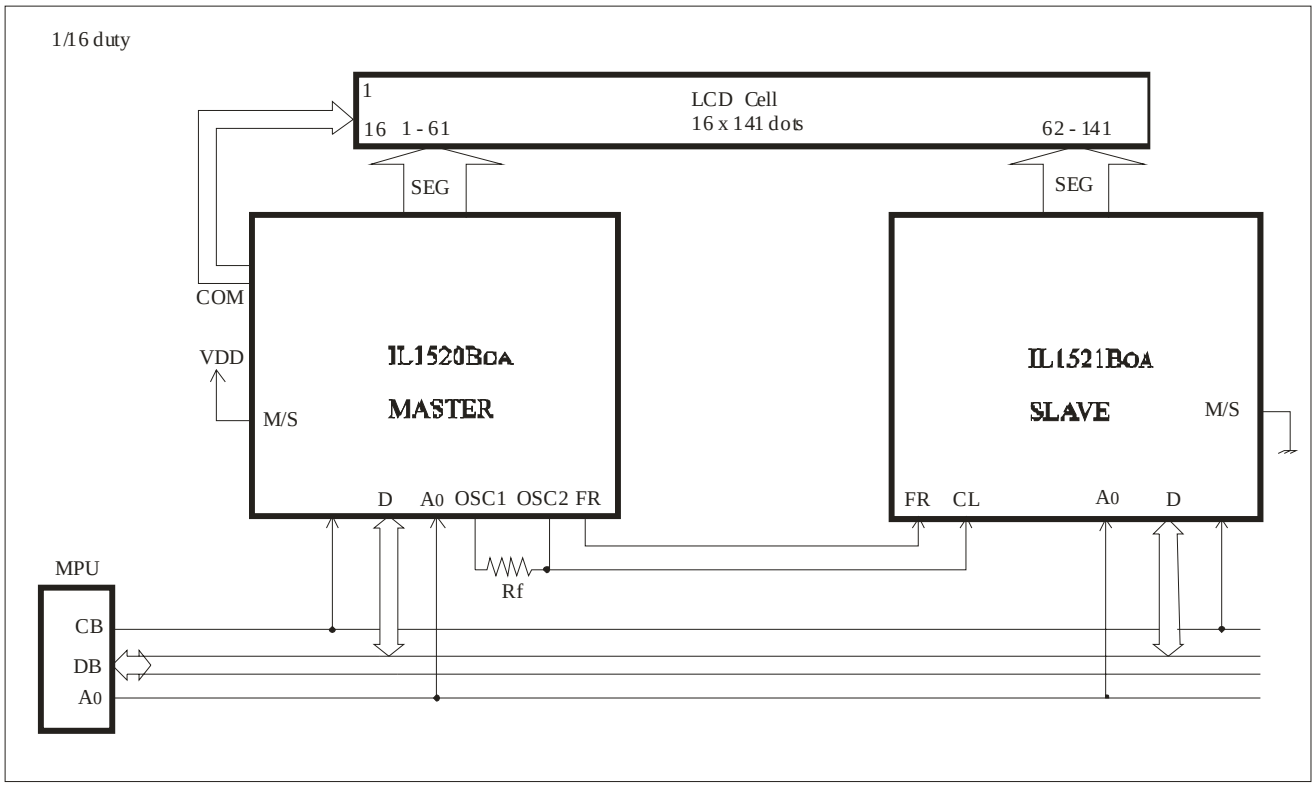
Note: Power Save mode is entered by selecting static drive in the Display OFF status.

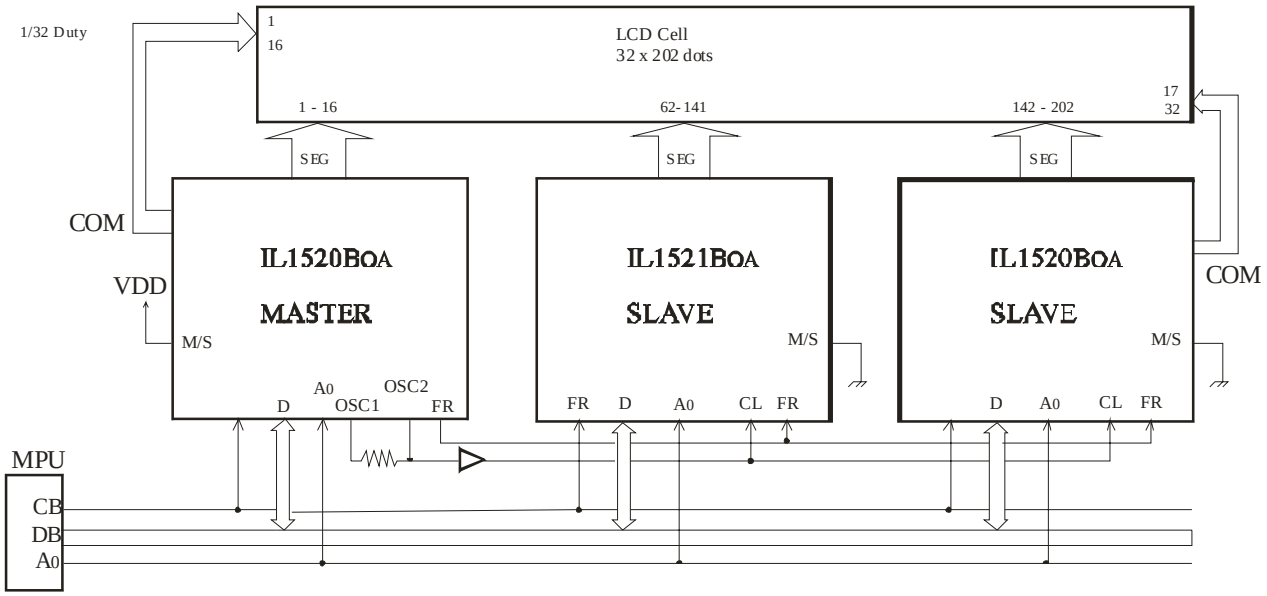
REFERENCE CIRCUITRY EXAMPLES

- **16 x 61 dots**



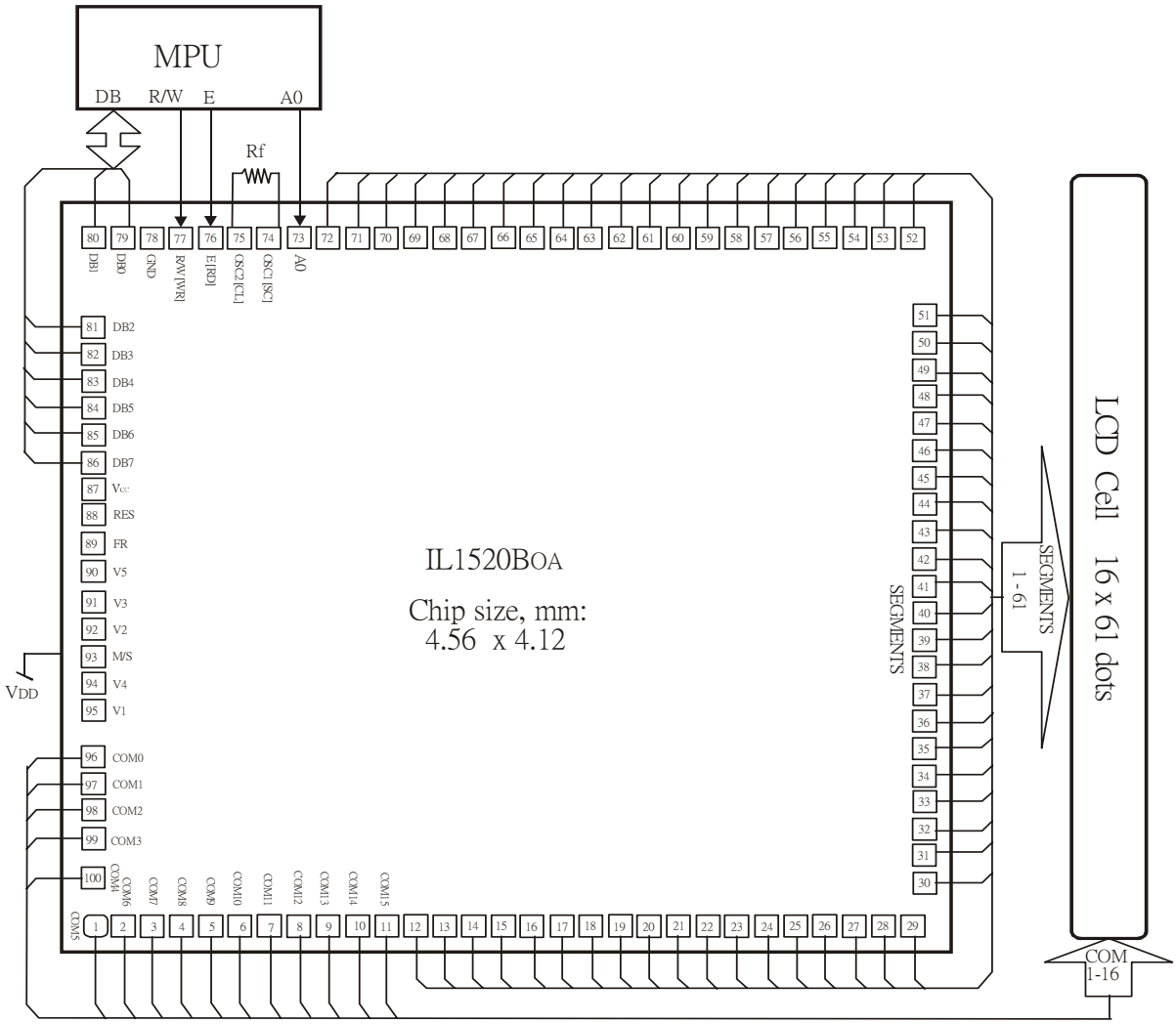
- **16 x 141 dots**



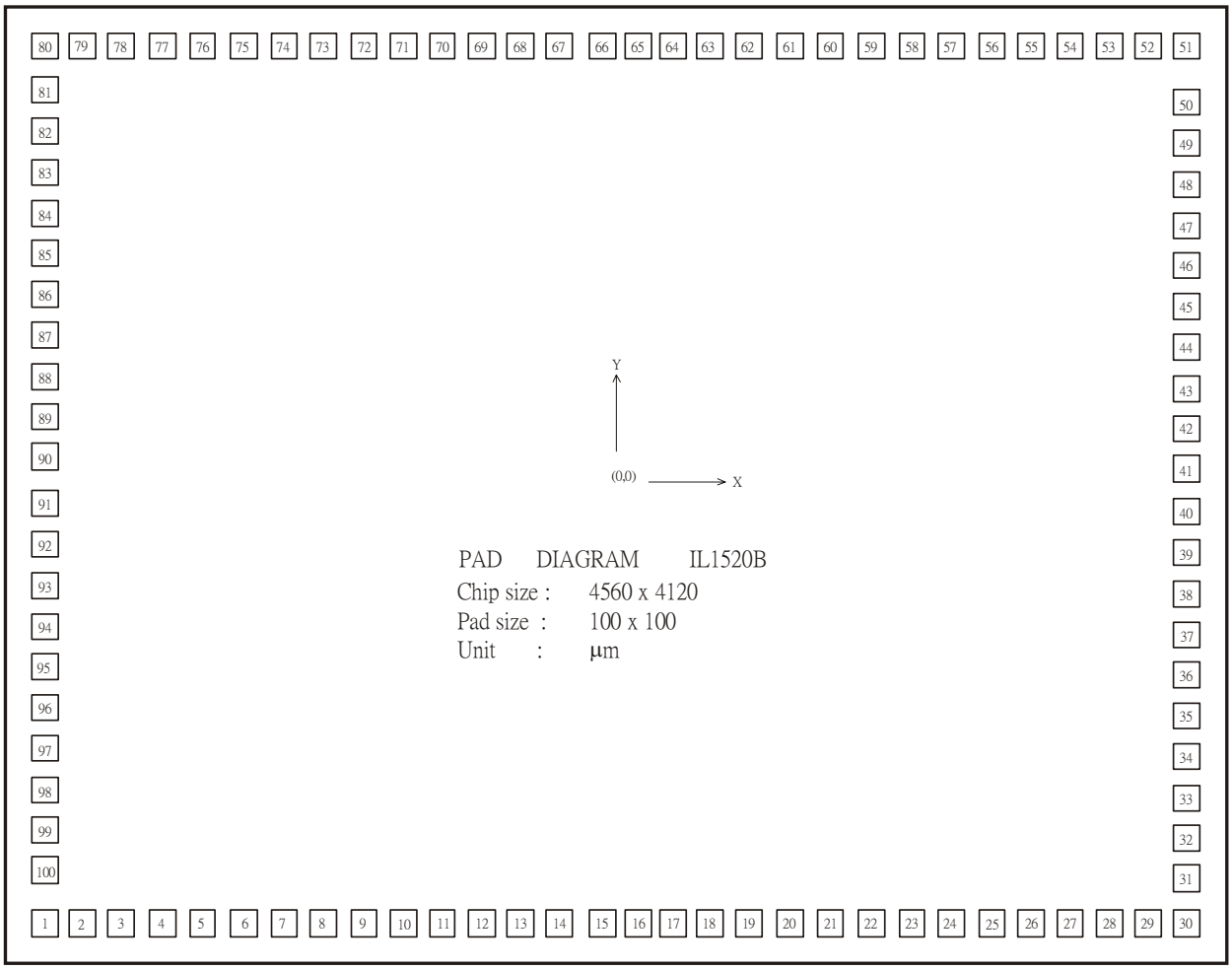


Note: If a system has two or more slave drivers a CMOS buffer will be required for clock signal.

APPLICATION CIRCUIT


MPU
DB
R/W
E
A0
Rf
IL1520BOA
Chip size, mm:
4.56 x 4.12
SEGMENTS
1 - 61
LCD Cell 16 x 61 dots
COM
1-16
VDD
DB1
DB0
GND
R/W [WR]
E [RD]
OSC2 [CL]
OSC1 [SC]
A0
DB2
DB3
DB4
DB5
DB6
DB7
Vcc
RES
FR
V5
V3
V2
M/S
V4
V1
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15

PAD LAYOUT


80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51
81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100
50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
Y
(0,0)
X
PAD DIAGRAM IL1520B
Chip size : 4560 x 4120
Pad size : 100 x 100
Unit : μm

PAD LOCATION

Pad size 100x100 (Unit: μm)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM5	-2099	-1908	35	SEG37	2129	-923	69	SEG3	-479	1908
2	COM6	-1979	-1908	36	SEG36	2129	-773	70	SEG2	-629	1908
3	COM7	-1829	-1908	37	SEG35	2129	-623	71	SEG1	-779	1908
4	COM8	-1679	-1908	38	SEG34	2129	-473	72	SEG0	-929	1908
5	COM9	-1529	-1908	39	SEG33	2129	-323	73	A0	-1079	1908
6	COM10	-1379	-1908	40	SEG32	2129	-173	74	OSC1 [CS]	-1229	1908
7	COM11	-1229	-1908	41	SEG31	2129	-23	75	OSC2 [CL]	-1379	1908
8	COM12	-1079	-1908	42	SEG30	2129	127	76	E [RD]	-1529	1908
9	COM13	-929	-1908	43	SEG29	2129	277	77	R/W (WR)	-1679	1908
10	COM14	-779	-1908	44	SEG28	2129	427	78	GND	-1829	1908
11	COM15	-629	-1908	45	SEG27	2129	577	79	DB0	-1979	1908
12	SEG60	-479	-1908	46	SEG26	2129	727	80	DB1	-2129	1908
13	SEG59	-329	-1908	47	SEG25	2129	877	81	DB2	-2129	1413
14	SEG58	-179	-1908	48	SEG24	2129	1027	82	DB3	-2129	1263
15	SEG57	-29	-1908	49	SEG23	2129	1177	83	DB4	-2129	1113
16	SEG56	121	-1908	50	SEG22	2129	1327	84	DB5	-2129	963
17	SEG55	271	-1908	51	SEG21	2129	1477	85	DB6	-2129	813
18	SEG54	421	-1908	52	SEG20	2071	1908	86	DB7	-2129	663
19	SEG53	571	-1908	53	SEG19	1921	1908	87	V_{CC}	-2129	512
20	SEG52	721	-1908	54	SEG18	1771	1908	88	RES	-2129	362
21	SEG51	871	-1908	55	SEG17	1621	1908	89	FR	-2129	212
22	SEG50	1021	-1908	56	SEG16	1471	1908	90	V5	-2129	62
23	SEG49	1171	-1908	57	SEG15	1321	1908	91	V3	-2129	-112
24	SEG48	1321	-1908	58	SEG14	1171	1908	92	V2	-2129	-262
25	SEG47	1471	-1908	59	SEG13	1021	1908	93	M/S	-2129	-412
26	SEG46	1621	-1908	60	SEG12	871	1908	94	V4	-2129	-562
27	SEG45	1771	-1908	61	SEG11	721	1908	95	V1	-2129	-712
28	SEG44	1921	-1908	62	SEG10	571	1908	96	COM0	-2129	-967
29	SEG43	2071	-1908	63	SEG9	421	1908	97	COM1	-2129	-1117
30	SEG42	2129	-1673	64	SEG8	271	1908	98	COM2	-2129	-1267
31	SEG41	2129	-1523	65	SEG7	121	1908	99	COM3	-2129	-1422
32	SEG40	2129	-1373	66	SEG6	-29	1908	100	COM4	-2129	-1640
33	SEG39	2129	-1223	67	SEG5	-179	1908				
34	SEG38	2129	-1073	68	SEG4	-329	1908				

Note: Pads 74,75 are OSC1, OSC2 for IL1520B $_{OA}$ and CS, CL for IL1520B $_{AA}$ respectively. All other pad names are identical.